[(<002611_C1>)] , , Ring 1

Verse 1 [<TB>] : According to Moore's law statement,

[<$>] After 2 years the number of transistors on the chip will double

Sentence 2 [<DE>]: In what year was the IAS (Institute for Advanced Studies) computer started?

[<$>] 1947

Verse 3 [<TB>]: The first computer ENIAC with memory

[<$>] Contains only data

Verse 4 [<DE>]: According to the Von Newmann principle, the installation of data into the computer is done by:

[<$>]Electric impulse

Question 5 [<KH>]: The first computer ENIAC was capable of doing

[<$>] 5000 additions per second

Question 6 [<TB>]: The IAS (Institute for Advanced Studies) computer is programmed according to the method:

[<$>] Based on von Neumann/Turing principle

Question 7 [<TB>]: Which of the following components did the first ENIAC use?

[<$>] Electronic lamp

Question 8 [<TB>]: According to Von Newmann's principle

[<$>] Memory is address-by-cell, independent of its contents

Question 9 [<TB>] : An example of a computer firmware is:

[<$>] ROM BIOS driver program

Question 10 [<DE>]: The first generation of computers is called the generation

[<$>] The computer uses an electronic vacuum lamp

Question 11 [<TB>]: What is an electronic computer?

[<$>] Information storage device

Question 12 [<TB>]: Which of the following statements belongs to Von Newmann's principle?

[<$>] Addressed computer memory

Question 13 [<DE>]: The fourth generation of computers is called the generation

[<$>] Computers using microchips VLSI

Question 14 [<TB>]: The computer's software is:

[<$>] Program is installed in ROM memory

Question 15 [<TB>]: Choose the correct answer from the following options:

[<$>] Turing machine consists of a finite state controller, a write tape, and a read/write head

Question 16 [<KH>]: According to the Von Newmann principle, the CU control unit executes instructions in steps

[<$>] Receive instruction from memory, decode and execute instruction sequentially

Question 17 [<KH>]: According to Von Newmann's principle, to change the order in which instructions are executed, we just need:

[<$>] Change the contents of the instruction pointer register with the address of the instruction to be executed

Question 18 [<DE>]: The third generation of computers is called the generation

[<$>] Computers using SSI, MSI, LSI

Question 19 [<TB>]: People evaluate the development of digital electronic computers through the stages based on which of the following criteria?

[<$>] All 3 criteria above

Question 20 [<TB>]: IAS computers have memory

[<$>] Contains program and data

Question 21 [<KH>]: The first computer ENIAC was programmed according to the method:

[<$>] Set the position of the switches and cables

Question 22 [<TB>]: What is firmware in computers?

[<$>] Software placed inside electronic circuits during manufacturing

Question 23 [<KH>]: The program is

[<$>] A sequence of instructions stored in memory that tells the computer to do a specific job.

Question 24 [<TB>]: Which of the following statements is correct?

[<$>] Computer hardware includes physical objects such as: mainboard, RAM, ROM, hard disk, monitor

Question 25 [<DE>]: The IBM-702 computer was born in

[<$>] 1955

Question 26 [<DE>]: The IBM-701 computer was born in

[<$>] 1953

Question 27 [<TB>]: One of the contents of Von Newmann's principle is:

[<$>] The computer can operate according to a stored program

Question 28 [<DE>]: When was the first computer ENIAC completed?

[<$>] 1946

Question 29 [<TB>]: Classification of computers according to the criteria of purpose of use are classified into types?

[<$>] Personal computers, servers, embedded computers

Question 30 [<KH>]: The second generation of computers is called the generation

[<$>] Transistor computers

Question 31 [<KH>]: High-level languages were born at the same time as which generation of computers?

[<$>] Second Generation: Transistor Computers (1960s)

Question 32 [<DE>]: The history of computer development to this day has gone through several stages

[<$>] 5 stages

Question 33 [<TB>]: Which of the following statements belongs to the content of Von Newmann's principle?

[<$>] The computer uses a program counter to indicate the position of the next instruction

Question 34 [<KH>]: The first computer ENIAC had

[<$>] 1800 electronic lights and 1500 relays

Question 35 [<DE>]: The first microprocessor Intel 4004 was born in

[<$>] 1971

Question 36 [<TB>]: Which of the following statements is not part of Von Newmann's principle?

[<$>] Each instruction must have a memory location containing the address of the next instruction

Question 37 [<KH>]: The fifth generation of computers is called the generation

[<$>] Computers using ULSI ICs, SoC

Question 38 [<KH>]: According to Von Newmann's principle, to access a block of data, we need:

[<$>] Specifies the address of the data block

Question 39 [<TB>]: The basic components of a computer include:

[<$>] Memory, CPU, BUS, I/O and Peripherals

[(<002611_C2>)] , , Chapter 2

Question 1 [<KH>] : Which of the following statements is false?

[<$>] The instruction set architecture of a computer includes instructions, data types, and working modes

Question 2 [<DE>] : Which of the following statements is incorrect?

[<$>] Every new form of computer organization must come with a new instruction set architecture.

Question 3 [<TB>] : Which of the following statements is true?

[<$>] The instruction set architecture (Instruction Set Architecture) changes slowly and the computer organization (Computer Organization) changes very quickly.

Question 4 [<TB>] : Considering the instruction set of the computer, which of the following statements is true:

[<$>] Each processor has a defined instruction set

[(<002611_C3>)] , , Ring 3

Question 1 [<TB>]: Decimal -127 $_{(10)}$ corresponds to which of the following 8-bit signed binary numbers (two's complement code):

[<$>] 1000 0001 $_{(2)}$

Question 2 [<TB>] : In the hexadecimal numbering system (Hexa), the number 5CD7 (16) corresponds to which of the following decimal values:

[<$>] 23767 (10)

Question 3 [<TB>] : The binary number 1100 1011 1101 (2) corresponds to which of the following hexadecimal (Hexa) values:

[<$>] CBD (16)

Question 4 [<TB>]: The sum of two unsigned, 8-bit binary numbers 0101 0101 (2) and 0110 1001 (2) equals which of the following binary numbers:

[<$>] 1011 1110 (2)

Question 5 [<TB>] : Out of the 80-bit floating point representation in computers, how many bits is the exponent component?

[<$>] 15 bits

Question 6 [<TB>]: For the IEEE 754/85 standard on the representation of double-extended real numbers, the length is:

[<$>] 80 bits

Question 7 [<DE>]: How many characters does the extended ASSCII encoder contain?

[<$>] 256

Question 8 [<DE>]: In the information transmission system of a computer divided by bus function, what types of buses are there?

[<$>] There are 3 types of bus: data bus; address bus; control bus.

Question 9 [<TB>]: The number 1101 0011 1101 (2) corresponds to which of the following decimal values:

[<$>] 3389 (10)

Question 10 [<TB>]: In the binary number system 11001.101 (2) corresponds to which of the following decimal values:

[<$>] 25.625

Question 11 [<TB>]: The number 157 $_{(10)}$ corresponds to which of the following binary values:

   [<$>] 10011101 $_{(2)}$

Question 12 [<TB>]: The number 222.5 $_{(10)}$ corresponds to which of the following binary values:

   [<$>] 11011110.1000 $_{(2)}$

Question 13 [<TB>]: Among the 32-bit floating point representation in computers, how many bits are the mantissa?

   [<$>] 23 bits

Question 14 [<TB>]: In the computer representation for integers with the addition sign, the result is false when:

   [<$>] Adding two terms with the same sign gives the sum of the opposite signs of the two terms

Question 15 [<TB>]: The program counter PC(Program Counter) will automatically increase to point to the next instruction:

   [<$>] After the instruction is loaded into the instruction register IR(Instruction Register).

Question 16 [<TB>]: The number 277 $_{(10)}$ corresponds to which of the following binary values:

   [<$>] 100010101 $_{(2)}$

Question 17 [<TB>]: What is the BCD code?

   [<$>] Code that uses binary bits to represent decimal digits

Question 18 [<TB>]: Out of the 64-bit floating-point representation in the computer, how many bits is the sign element?

   [<$>] 1 bit

Question 19 [<TB>]: The difference between two 8-bit unsigned binary numbers 0110 1011 $_{(2)}$ and 0101 0101 $_{(2)}$ is equal to which of the following binary numbers:

[<$>] 0001 0110 $_{(2)}$

Question 20 [<DE>]: Out of the 32-bit floating point representation in the computer, how many bits are the sign components?

[<$>] 1 bit

Question 21 [<TB>]: An 8-bit signed binary number (two's complement code) 1111 0011 $_{(2)}$ corresponds to which of the following decimals:

[<$>] -13 $_{(10)}$

Question 22 [<TB>]: In the hexadecimal numbering system (Hexa), the number 5F4B $_{(16)}$ corresponds to which of the following binary values:

[<$>] 0101 1111 0100 1011 $_{(2)}$

Question 23 [<TB>]: In the binary system 11101.01 $_{(2)}$ corresponds to which of the following decimal values:

[<$>] 29.25

Question 24 [<DE>]: Main memory is memory:

[<$>] RAM ((Random Access Memory)

Question 25 [<DE>]: Which of the following parts is not part of the central processing unit:

[<$>] I/O unit

Question 26 [<TB>]: In the central processor, the component that connects the CU, ALU and registers is called:

[<$>] Internal bus

Question 27 [<KH>]: In the computer representation for signed integers, the 8-bit addition of 91 + 63 gives the result:

[<$>] -102

[(<002611_C3>)] , , Ring 3

Question 28 [<KH>]: The difference between two unsigned, 8-bit binary numbers 0110 1011 $_{(2)}$ and 0101 0111 $_{(2)}$ is equal to which of the following binary numbers:

[<$>] 0001 0100 $_{(2)}$

Question 29 [<KH>]: The product of two unsigned, 8-bit binary numbers 0000 1101 $_{(2)}$ and 0000 1011 $_{(2)}$ equals which of the following binary numbers:

[<$>] 1000 1111 $_{(2)}$

Question 30 [<KH>]: The quotient of two unsigned, 8-bit binary numbers 0110 0011 $_{(2)}$ and 0000 1101 $_{(2)}$ whose quotient and remainder are equal to which of the following pairs of binary numbers:

[<$>] Trade: 0111 $_{(2)}$, balance: 1000 $_{(2)}$

Question 31 [<DE>]: The input-output system includes

[<$>] Peripherals, I/O modules

Question 32 [<DE>]: What unit is the system clock speed measured in?

[<$>] Hz

Question 33 [<TB>]: In the computer representation for signed integers ,8 bit subtraction 67 -91 gives the result:

[<$>] -24

Question 34 [<TB>]: The number 227,3125 $_{(10)}$ corresponds to which of the following binary values:

[<$>] 11100011.0101 $_{(2)}$

Question 35 [<TB>]: The number 1111 0101 1010 $_{(2)}$ corresponds to which of the following decimal values:

[<$>] 3930 $_{(10)}$

Question 36 [<KH>]: For IEEE 754/85 standard on representation of single real numbers, give the following representation: C2 82 80 00 (H) . Its decimal value is:

   [<$>] -65.25

Question 37 [<TB>]: In the hexadecimal numbering system (Hexa), the number 345F (16) corresponds to which of the following decimal values:

   [<$>] 13407 (10)

Question 38 [<TB>]: In the decimal numbering system the number 13779 (10) corresponds to which of the following hexadecimal (Hexa) values:

   [<$>] 35D3 (16)

Question 39 [<KH>]: For the IEEE 754/85 standard on the representation of single real numbers, the representation of real numbers 73,625 is:

   [<$>] 42 93 40 00 (H) Or 01000010 10010011 01000000 00000000 (2)

Question 40 [<TB>]: In the hexadecimal (Hexa) numbering system, the number 5B7D (16) corresponds to which of the following binary values:

   [<$>] 0101 1011 0111 1101 (2)

Question 41 [<TB>]: Types of interrupts in computers are:

   [<$>] Interrupt due to program execution error; interrupt due to hardware failure; interrupt because the I/O module sends an interrupt signal to the CPU requesting data exchange.

Question 42 [<TB>]: The binary number 1101 0011 1001 (2) corresponds to which of the following hexadecimal (Hexa) values:

   [<$>] D39 (16)

Question 43 [<TB>]: In the binary system the number 10111.10 (2) corresponds to which of the following decimal values:

   [<$>] 23.5

Question 44 [<DE>]: Main Memory

   [<$>] Contains programs and data being used by the CPU

Question 45 [<TB>]: In the hexadecimal (Hexa) numbering system, the number 3CF5 $_{(16)}$ corresponds to which of the following decimal values:

[<$>] 15605 $_{(10)}$

Question 46 [<KH>]: In the computer representation for signed integers, 8-bit addition -91 + 53 gives the result:

[<$>] -38

Question 47 [<TB>]: In the computer representation for signed integers which statement is false:

[<$>] Adding two numbers with the same sign is always correct

Question 48 [<KH>]: The instruction execution cycle of the computer includes

[<$>] 4 main steps (get instruction address, load instruction code, decode instruction, execute instruction)

Question 49 [<TB>]: Processor speed

[<$>] Indirectly evaluated through processor clock frequency

Question 50 [<TB>]: The number 267 $_{(10)}$ corresponds to which of the following binary values:

[<$>] 100001011 $_{(2)}$

Question 51 [<TB>]: The decimal -105 $_{(10)}$ corresponds to which of the following 8-bit signed binary numbers (two's complement code):

[<$>] 1001 0111 $_{(2)}$

Question 52 [<TB>]: The number 254.1875 $_{(10)}$ corresponds to which of the following binary values:

[<$>] 111111110.0011 $_{(2)}$

Question 53 [<TB>]: The number 234 $_{(10)}$ corresponds to which of the following binary values:

[<$>] 11101010 $_{(2)}$

Question 54 [<TB>]: Among the 32-bit floating-point representations in computers, how many bits are the sign components?

[<$>] 1 bit

Question 55 [<TB>]: The number 202,375 $_{(10)}$ corresponds to which of the following binary values:

[<$>] 11001010.0110 $_{(2)}$

Question 56 [<TB>]: Of the 64-bit floating point representations in computers, how many bits are the exponential components?

[<$>] 11 bits

Question 57 [<TB>]: In the decimal numbering system the number 15948 $_{(10)}$ corresponds to which of the following hexadecimal (Hexa) values:

[<$>] 3E4C $_{(16)}$

Question 58 [<TB>]: In the hexadecimal numbering system (Hexa), the number 5E8F $_{(16)}$ corresponds to which of the following decimal values:

[<$>] 24207 $_{(10)}$

Question 59 [<KH>]: For the IEEE 754/85 standard for representing single real numbers, the bits for fields (S+E+M) are:

[<$>] 1+8+23

Sentence 60 [<TB>]: An 8-bit signed binary number (2's complement code) 1011 1011 $_{(2)}$ corresponds to which of the following decimals:

[<$>] -69 $_{(10)}$

Question 61 [<TB>]: The number 1110 1111 1011 $_{(2)}$ corresponds to which of the following decimal values:

[<$>] 3835 $_{(10)}$

Question 62 [<KH>]: In the computer representation for signed integers, the 8-bit subtraction (-67) -91 results in:

[<$>] 98

Question 63 [<KH>]: The quotient of two unsigned, 8-bit binary numbers 0110 1011 $_{(2)}$ and 0000 1011 $_{(2)}$ whose quotient and remainder is equal to which of the following pairs of binary numbers:

  [<$>] quotient: 1001 $_{(2)}$, remainder: 1000 $_{(2)}$

Question 64 [<KH>]: For IEEE 754/85 standard on representation of real numbers (single), give the following representation: C2 BF 00 00 $_{(H)}$. Its decimal value is:

  [<$>] -95.5

Question 65 [<TB>]: The difference between two 8-bit unsigned binary numbers 0110 0011 $_{(2)}$ and 0101 0101 $_{(2)}$ is equal to which of the following binary numbers:

  [<$>] 0000 1110 $_{(2)}$

Question 66 [<TB>]: The difference between two 8-bit unsigned binary numbers 0110 1001 $_{(2)}$ and 0100 1101 $_{(2)}$ is equal to which of the following binary numbers:

  [<$>] 0001 1100 $_{(2)}$

Question 67 [<TB>]: The product of two unsigned, 8-bit binary numbers 0000 1110 $_{(2)}$ and 0000 1010 $_{(2)}$ equals which of the following binary numbers:

  [<$>] 1000 1100 $_{(2)}$

Question 68 [<TB>]: In the information transmission system of a computer divided by the bus speed hierarchy in the computer, what types of buses are there?

  [<$>] There are 3 types of bus: bus inside microprocessor; main memory bus; in-out bus

Question 69 [<TB>]: Which of the following parts is not part of the central processing unit:

  [<$>] Internal Memory

Question 70 [<DE>]: Information is stored and transmitted inside the computer in the form of:

[<$>] Binary

Question 71 [<TB>]: The number 1101 1011 1000 $_{(2)}$ corresponds to which of the following decimal values:

[<$>] 3512 $_{(10)}$

Question 72 [<TB>]: The sum of two unsigned, 8-bit binary numbers 0101 1101 $_{(2)}$ and 0110 1011 $_{(2)}$ equals which of the following binary numbers:

[<$>] 1100 1000 $_{(2)}$

Question 73 [<TB>]: The number 1010 0011 1101 $_{(2)}$ corresponds to which of the following decimal values:

[<$>] 2621 $_{(10)}$

Question 74 [<TB>]: In the binary number system 11101.11 $_{(2)}$ corresponds to which of the following decimal values:

[<$>] 29.75

Question 75 [<KH>]: How many bits does the BCD code represent for each decimal digit?

[<$>] 4 bits

Question 76 [<KH>]: For IEEE 754/85 standard on the representation of single real numbers, the representation of real numbers -53.125 is:

[<$>] C2 54 80 00 $_{(H)}$ Or 11000010 01010100 10000000 00000000 $_{(2)}$

Question 77 [<DE>]: How many bits are encoded in the standard ASSCII encoder?

[<$>] 7 bits

Question 78 [<KH>]: A microprocessor takes an average of 4 frequency cycles for each operation. Knowing the processor has a clock speed of 2Ghz, so each machine operation will take the amount of time to perform:

[<$>] 2.0ns

Question 79 [<DE>]: Which of the following parts is not part of the central processing unit:

[<$>] System BUS (system BUS)

Question 80 [<KH>]: The product of two unsigned, 8-bit binary numbers 0000 0110 $_{(2)}$ and 0000 1011 $_{(2)}$ equals which of the following binary numbers:

[<$>] 0100 0010 $_{(2)}$

Question 81 [<TB>]: The sum of two unsigned, 8-bit binary numbers 0101 0111 $_{(2)}$ and 0110 1011 $_{(2)}$ equals which of the following binary numbers:

[<$>] 1100 0010 $_{(2)}$

Question 82 [<TB>]: Out of the 32-bit floating point representation in computers, how many bits is the exponent component?

[<$>] 8 bits

Question 83 [<KH>]: For the IEEE 754/85 standard for representing real numbers in double (double) the bits for fields (S+E+M) are:

[<$>] 1+11+52

Question 84 [<TB>]: The decimal number -54 $_{(10)}$ corresponds to which of the following 8-bit signed binary numbers (two's complement code):

[<$>] 1100 1010 $_{(2)}$

Question 85 [<TB>]: The sum of two unsigned, 8-bit binary numbers 0101 0101 $_{(2)}$ and 0110 1011 $_{(2)}$ equals which of the following binary numbers:

[<$>] 1100 0000 $_{(2)}$

Question 86 [<TB>]: The number 186,875 $_{(10)}$ corresponds to which of the following binary values:

[<$>] 10111010.1110 $_{(2)}$

Question 87 [<TB>]: The number 1110 0011 1100 $_{(2)}$ corresponds to which of the following decimal values:

[<$>] 3644 $_{(10)}$

Question 88 [<TB>]: The number 239.6875 $_{(10)}$ corresponds to which of the following binary values:

[<$>] 11101111.1011 $_{(2)}$

Question 89 [<TB>]: In the hexadecimal numbering system (Hexa), the number 5F4B $_{(16)}$ corresponds to which of the following decimal values:

[<$>] 24395 $_{(10)}$

Question 90 [<TB>]: Among the 80-bit floating-point representation in computers, how many bits are the mantissa?

[<$>] 64 bit

Question 91 [<TB>]: The binary number 1010 0011 1101 $_{(2)}$ corresponds to which of the following hexadecimal (Hexa) values:

[<$>] A3D $_{(16)}$

Question 92 [<KH>]: For the IEEE 754/85 standard on the representation of single real numbers, the representation of real numbers 101.25 is:

[<$>] 42 CA 80 00 $_{(H)}$ Or 01000010 11001010 10000000 00000000 $_{(2)}$

Question 93 [<TB>]: In the binary system 10101.11 $_{(2)}$ corresponds to which of the following decimal values:

[<$>] 21.75

Question 94 [<DE>]: In the binary number system 11001.10 $_{(2)}$ corresponds to which of the following decimal values:

[<$>] 25.50

Question 95 [<KH>]: In the computer representation for signed integers, the 8-bit principle of subtraction is:

[<$>] Change the sign of the minus number and then add the two signed integers.

Question 96 [<TB>]: The difference between two 8-bit unsigned binary numbers 0110 1001 $_{(2)}$ and 0101 0101 $_{(2)}$ is equal to which of the following binary numbers:

[<$>] 0001 0100 (2)

Question 97 [<DE>]: In the hexadecimal (Hexa) numbering system, the number 34F5 (16) corresponds to which of the following binary values:

[<$>] 0011 0100 1111 0101 (2)

Question 98 [<KH>]: How many bits are encoded in the extended ASSCII encoder?

[<$>] 8 bits

Question 99 [<DE>]: The number 227 (10) corresponds to which of the following binary values:

[<$>] 11100011 (2)

Question 100 [<TB>]: In the binary numbering system, the value of each number depends on:

[<$>] The digit itself and its position

Question 101 [<TB>]: Each input-output module has

[<$>] Have one or several I/O ports

Question 102 [<DE>]: Cache Memory

[<$>] Is SRAM memory

Question 103 [<KH>]: The decimal number -129 (10) corresponds to which of the following 8-bit signed binary numbers (two's complement code):

[<$>] Can't perform

Question 104 [<DE>]: In the hexadecimal numbering system (Hexa), the number 34F5 (16) corresponds to which of the following decimal values:

[<$>] 13557 (10)

Question 105 [<KH>]: The product of two unsigned, 8-bit binary numbers 0000 1101 (2) and 0000 1010 (2) equals which of the following binary numbers:

[<$>] 1000 0010 (2)

Question 106 [<KH>]: The quotient of two unsigned, 8-bit binary numbers 0101 0111 $_{(2)}$ and 0000 1011 $_{(2)}$ whose quotient and remainder is equal to which of the following pairs of binary numbers:

[<$>] quotient: 0111 $_{(2)}$, residual: 1010 $_{(2)}$

Question 107 [<TB>]: How many types of control signals are there in the memory module connection?

[<$>] There are two types of control signals, read and write (Read/Write).

Question 108 [<TB>]: In the information transmission system of a computer divided by the mode of operation of the bus in the computer, what types of buses are there?

[<$>] There are two types of bus: synchronous bus; asynchronous bus

Question 109 [<TB>]: For the IEEE 754/85 standard for the representation of a single real number of length:

[<$>] 32 bits

Question 110 [<DE>]: The number 247 $_{(10)}$ corresponds to which of the following binary values:

[<$>] 11110111 $_{(2)}$

Question 111 [<KH>]: In the computer representation for signed integers, 8-bit addition (-39) + (-42) results in:

[<$>] -81

Question 112 [<KH>]: For IEEE 754/85 standard on the representation of real numbers (single), the representation is as follows: 42 15 00 00 $_{(H)}$. Its decimal value is:

[<$>] 37.25

Question 113 [<KH>]: How many bits does the EBCDIC code represent for each character?

[<$>] 8 bits

Question 114 [<DE>]: In the decimal numbering system 15078 $_{(10)}$ corresponds to which of the following hexadecimal (Hexa) values:

[<$>] 3AE6 $_{(16)}$

Question 115 [<DE>]: The number 1001 1111 1001 $_{(2)}$ corresponds to which of the following decimal values:

[<$>] 2553 $_{(10)}$

Question 116 [<DE>]: Which of the following is the computer's internal memory?

[<$>] ROM, RAM, Cache

Question 117 **[<DE>]** : Which of the following parts belongs to the central processing unit:

[<$>] Set of general-purpose registers

Question 118 [<KH>]: The product of two unsigned, 8-bit binary numbers 0000 1110 $_{(2)}$ and 0000 1011 $_{(2)}$ equals which of the following binary numbers:

[<$>] 1001 1010 $_{(2)}$

Question 119 [<DE>]: The sum of two unsigned, 8-bit binary numbers 0100 1101 $_{(2)}$ and 0110 1001 $_{(2)}$ equals which of the following binary numbers:

[<$>] 1011 0110 $_{(2)}$

Question 120 [<TB>]: Of the 64-bit floating point representations in computers, how many bits are the mantissa?

[<$>] 52 bits

Question 121 [<KH>]: For the IEEE 754/85 standard on the representation of single real numbers, the representation of real numbers -119.5 is:

[<$>] C2 EF 00 00 $_{(H)}$ Or 11000010 11101111 00000000 00000000 $_{(2)}$

Question 122 [<DE>]: The decimal number -29 $_{(10)}$ corresponds to which of the following 8-bit signed binary numbers (two's complement code):

[<$>] 1110 0011 $_{(2)}$

Question 123 [<DE>]: The sum of two unsigned, 8-bit binary numbers 0101 0101 $_{(2)}$ and 0110 0011 $_{(2)}$ equals which of the following binary numbers:

[<$>] 1011 1000 $_{(2)}$

Question 124 [<DE>]: The number 154,9375 $_{(10)}$ corresponds to which of the following binary values:

[<$>] 10011010.1111 $_{(2)}$

Question 125 [<DE>]: The number 1100 1011 1100 $_{(2)}$ corresponds to which of the following decimal values:

[<$>] 3260 $_{(10)}$

Question 126 [<DE>]: The number 199.5625 $_{(10)}$ corresponds to which of the following binary values:

[<$>] 11000111,1001 $_{(2)}$

Question 127 [<DE>]: In the hexadecimal (Hexa) numbering system, the number 5B7D $_{(16)}$ corresponds to which of the following decimal values:

[<$>] 23421 $_{(10)}$

Question 128 [<TB>]: Of the floating point representations of 80 bits in computers, how many bits are in the sign element?

[<$>] 1 bit

Question 129 [<DE>]: The binary number 1110 0011 1100 $_{(2)}$ corresponds to which of the following hexadecimal (Hexa) values:

[<$>] E3C $_{(16)}$

Question 130 [<KH>]: For IEEE 754/85 standard on representation of single real numbers (single), give the following representation: 42 22 80 00 $_{(H)}$. Its decimal value is:

[<$>] 40.625

Question 131 [<DE>]: In the binary system 10101.01 $_{(2)}$ corresponds to which of the following decimal values:

[<$>] 21.25

Question 132 [<DE>]: In the binary number system 11001.011 $_{(2)}$ corresponds to which of the following decimal values:

[<$>] 25,375

Question 133 [<KH>]: For IEEE 754/85 standard on representation of real numbers in double (double) form of length:

[<$>] 64 bit

Question 134 [<DE>]: The difference between two 8-bit unsigned binary numbers 0110 1011 $_{(2)}$ and 0101 1101 $_{(2)}$ is equal to which of the following binary numbers:

[<$>] 0000 1010 $_{(2)}$

Question 135 [<DE>]: In the hexadecimal (Hexa) numbering system, the number 3CF5 $_{(16)}$ corresponds to which of the following binary values:

[<$>] 0011 1100 1111 0101 $_{(2)}$

Question 136 [<KH>]: In the computer representation for signed integers, 8-bit addition (-73) + (-86) results in

[<$>] 97

Question 137 [<DE>]: The number 218 $_{(10)}$ corresponds to which of the following binary values:

[<$>] 11011010 $_{(2)}$

Question 138 [<KH>]: According to IEEE754/85 standard, floating point real numbers have the form

[<$>] 32 bits; 44 bits; 64 bits; 80 bits

Question 139 [<KH>]: Please state the correct statement:

[<$>] Each I/O port is assigned a unique address and does not change every time the computer is started

Question 140 [<DE>]: Cache memory is usually divided into

[<$>] 3 levels

Question 141 [<DE>]: An 8-bit signed binary number (2's complement code) 1110 0010 $_{(2)}$ corresponds to which of the following decimals:

[<$>] -30 $_{(10)}$

Question 142 [<DE>]: In the hexadecimal numbering system (Hexa), the number 44C5 $_{(16)}$ corresponds to which of the following decimal values:

[<$>] 17605 $_{(10)}$

Question 143 [<KH>]: The quotient of two unsigned, 8-bit binary numbers 0110 1011 $_{(2)}$ and 0000 1101 $_{(2)}$ whose quotient and remainder is equal to which of the following pairs of binary numbers:

[<$>] quotient: 1000 $_{(2)}$, remainder: 0011 $_{(2)}$

Question 144 [<KH>]: The quotient of two unsigned, 8-bit binary numbers 0101 0111 $_{(2)}$ and 0000 1011 $_{(2)}$ whose quotient and remainder is equal to which of the following pairs of binary numbers:

[<$>] Trade: 0111 $_{(2)}$, balance: 0110 $_{(2)}$

Question 145 [<TB>]: How many types of control signals are there in the I/O module connection?

[<$>] There are 3 types of control signals: Input, Output, and Interrupt.

Question 146 [<TB>]: The data exchange between the peripheral device and the computer is done via:

[<$>] One Gate

Question 147 [<KH>]: For the IEEE 754/85 standard for representing double-extended real numbers, the bits for fields (S+E+M) are:

[<$>] 1+15+64

Question 148 [<DE>]: The number 285 $_{(10)}$ corresponds to which of the following binary values:

[<$>] 100011101 $_{(2)}$

Question 149 [<KH>]: In the computer representation for signed integers, which statement is true:

[<$>] Subtracting two numbers with the same sign is always true

Question 150 [<KH>]: How many characters does the standard ASSCII codec include?

[<$>] 128

Question 151 [<TB>]: What are the characters added in the extended ASSCII codec?

[<$>] Characters created by computer manufacturers or software developers

Question 152 [<DE>]: In the decimal numbering system the number 17275 $_{(10)}$ corresponds to which of the following hexadecimal (Hexa) values:

[<$>] 437B $_{(16)}$

Question 153 [<DE>]: The number 1011 0111 1011 $_{(2)}$ corresponds to which of the following decimal values:

[<$>] 2939 $_{(10)}$

[(<002611_C4>)] , , Ring 4

Question 1 [<KH>]: For the control block (in the CPU), which of the following functions is correct:

[<$>] Increment the contents of the PC to point to the next instruction

Question 2 [<TB>]: What components does the EU block in a microprocessor consist of?

[<$>] Arithmetic and Logic Computing Unit (ALU), Control Unit (CU) and Registers (RF)

Question 3 [<TB>]: Considering the control signals from the system bus to the CPU, which of the following statements is true:

[<$>] Interrupt request signal

Question 4 [<DE>]: The processor receives the command at:

[<$>] Memory

Sentence 5 [<TB>]: For the null flag Zero – ZF in the status register (in the CPU), its meaning is:

[<$>] Set to 1 when the result of the operation is 0

Question 6 [<TB>]: Considering the control signals inside the CPU, which of the following statements is true:

[<$>] Controls data transfer from register to ALU

Question 7 [<TB>]: For the carry flag - CF in the status register (in the CPU), which of the following statements is true:

[<$>] Set to 1 if the operation remembers out the highest bit

Question 8 [<KH>]: For machine code instructions, the operands can be:

[<$>] Source operand or destination operand or both source and destination operands or no operand

Question 9 [<TB>]: For a stack, which of the following statements is false:

[<$>] Is a FIFO (First In - First Out) structured memory area.

Question 10 [<DE>]: For machine code instructions, which of the following statements is false:

[<$>] Operand indicating the operation to be performed

Question 11 [<TB>]: For data registers (in the CPU), which of the following statements is false:

[<$>] Contains only the data of the stack memory

Question 12 [<TB>]: Considering the process of receiving data of the CPU, the order of execution is:

[<$>] Address -> Storage -> Register Set

Question 13 [<KH>]: For the control block (in the CPU), which of the following statements is true:

[<$>] Decode the instruction transferred from the instruction register to

Question 14 [<DE>]: For registers (in the CPU), which of the following statements is false:

[<$>] The programmer can change all the contents of the registers

Question 15 [<DE>]: For address registers (in the CPU), which of the following statements is false:

[<$>] Instruction area without management register

Question 16 [<TB>]: For example, the instruction is divided into 6 stages and the execution time of an instruction is 6T, if executing the instruction according to the Superpipeline architecture (Superpipeline & Hyperpipeline), the execution time of n instructions will be how much?

[<$>](6+n-1)T

Question 17 [<KH>]: Considering the execution stages of a processor instruction, which order is correct?

[<$>] Receive command -> Decode instruction -> Receive data -> Process data -> Write data

Question 18 [<DE>]: For a machine code instruction consisting of one operand, which of the following statements is true:

[<$>] One operand specified in the instruction can be the source operand or it can be the destination operand, and the other operand is the implicit operand.

Question 19 [<DE>]: For registers (in the CPU), which of the following statements is true:

[<$>] There are two types of registers (programmable registers and non-programmable registers)

Question 20 [<TB>]: What is the function of a microprocessor in a computer?

[<$>] Reads data from memory, processes each instruction, and writes results to memory or a peripheral device

Question 21 [<KH>]: Which of the following is not a characteristic of RISC computers:

[<$>] Multiple ways of executing instructions through multiple addressing modes

Question 22 [<TB>]: For the control block (in the CPU), which of the following functions is false:

[<$>] Logical operations

Question 23 [<DE>]: For the status register (in the CPU), which of the following statements is true:

[<$>] Contains control flags

Question 24 [<TB>]: For the stack pointer register SP - Stack Pointer (in CPU), which of the following statements is false:

[<$>] The stack pointer always points to the bottom of the stack

Question 25 [<DE>]: For a machine code instruction consisting of 3 operands, which of the following statements is true:

[<$>] Two source operands, one destination operand

Question 26 [<KH>]: The processor receives data at:

[<$>] Memory or Peripheral Device

Question 27 [<DE>]: For the -ALU arithmetic and logic block (in CPU), which of the following statements is true:

[<$>] Perform arithmetic operations and perform logical operations

Question 28 [<TB>]: Considering the process of receiving instructions from the CPU, the order of execution is:

[<$>] Program Counter->Memory -> Instruction Register

Question 29 [<TB>]: For the Overflow flag - OF in the status register (in the CPU), which of the following statements is true:

[<$>] Set to 1 when adding two integers with the same sign and the result has the opposite sign

Question 30 [<KH>]: Which of the following is not a characteristic of RISC computers:

[<$>] Variable length commands

Question 31 [<KH>]: For the program counter registers PC - Program Counter (in the CPU), which of the following statements is false:

[<$>] Contains code being executed

Question 32 [<TB>]: Considering the control signals from the system bus to the CPU, which of the following statements is false:

[<$>] The reply signal agrees to give way to the bus

Question 33 [<TB>]: For machine code instructions, which of the following statements is true:

[<$>] Machine instruction can have more than one operand

Question 34 [<DE>]: For registers (in the CPU), which of the following statements is false:

[<$>] Only one type of flag (Control Flag)

Question 35 [<TB>]: For the function of the control block (in the CPU), which of the following statements is false:

[<$>] Transport instruction from register to memory

Question 36 [<TB>]: For the Sign flag - SF in the status register (in the CPU), its meaning is:

[<$>] Set to 1 when the result of the operation is less than 0

Question 37 [<DE>]: For registers (in the CPU), which of the following is wrong to classify registers by function type:

[<$>] Address Register

Question 38 [<KH>]: Which of the following is not a characteristic of RISC computers:

[<$>] Multiple commands

Question 39 [<KH>]: Which of the following statements is false?

[<$>] The processor is composed of 2 components ALU and CU

Question 40 [<TB>]: Considering the control signals from the CPU to the system bus, which of the following statements is true:

[<$>] Memory cell read/write control

Question 41 [<KH>]: Considering the data processing stage of the CPU, the order of execution is:

[<$>] Arithmetic and Logic Calculator (ALU) -> Perform Math -> Data Register

Question 42 [<TB>]: For the carry flag - CF in the status register (in the CPU), which of the following statements is false:

[<$>] This is the overflow flag for numbers with

Question 43 [<TB>]: For the Overflow flag - OF in the status register (in the CPU), which of the following statements is false:

[<$>] Set to 1 when adding two integers with the same sign and the result has the same sign

Question 44 [<DE>]: For the ALU (in the CPU), which of the following statements is false:

[<$>] Perform square root

Question 45 [<TB>]: For address registers (in the CPU), which of the following statements is true:

[<$>] There are at least 3 types (Program counter – PC; Data pointer – DP; Stack pointer – SP)

Question 46 [<TB>]: Considering the process of writing (storing) data of the CPU, the order of execution is:

[<$>] Address -> Register Set -> Memory Cell

Question 47 [<KH>]: For data registers (in the CPU), which of the following statements is true:

[<$>] Contains temporary data or intermediate results

Question 48 [<DE>]: For registers (in the CPU), which of the following statements is true:

[<$>] There is a non-programmable register type

Question 49 [<TB>]: For data pointer registers DP - Data Pointer (in CPU), which of the following statements is true:

[<$>] Contains the address of the data memory location that the CPU wants to access

Question 50 [<TB>]: Considering the control signals inside the CPU, which of the following statements is false:

[<$>] Controls data transfer from CPU to register

Question 51 [<KH>]: Which of the following is not a characteristic of RISC computers:

[<$>] Many firmwares are used

Question 52 [<KH>]: Which of the following is not a part of a microprocessor?

[<$>] System Bus

Question 53 [<TB>]: For machine code instructions, which of the following statements is true:

[<$>] The instruction code in the machine instruction is unique

Question 54 [<DE>]: For a machine code instruction consisting of two operands, which of the following statements is true:

[<$>] One operand is both source and destination operand, the other is source operand

Question 55 [<KH>]: Considering the CPU instruction decoding stage, the order of execution is:

[<$>] Instruction register -> Control block -> Decode -> Control signal

Question 56 [<TB>]: The instruction pipeline architecture (Instruction Pipelining) is:

[<$>] Divide the instruction cycle into stages and allow overlapping execution

Question 57 [<TB>]: For the control block (in the CPU), which of the following functions is correct:

[<$>] Decode the instruction received from the instruction register to determine the operation required by the instruction

Question 58 [<TB>]: For the control block (in the CPU), which of the following statements is false:

[<$>] Drives only registers and the arithmetic and logic calculator (ALU)

Question 59 [<DE>]: To execute an instruction, the processor must go through:

[<$>] 5 stages

Question 60 [<TB>]: Considering the control signals from the CPU to the system bus, which of the following statements is false:

[<$>] Controls writing data to the register

[(<002611_C5>)] , , Ring 5

Question 1 [<KH>]: Given a computer with 256MB main memory capacity, 64KB Cache memory capacity, 64byte Line size, 4byte memory compartment length. In the case of the direct mapping technique of Tag + Line + Word address form emitted by the processor to access the Cache is:

[<$>] 12+11+4

Question 2 [<KH>]: With a SRAM memory chip with an address bus of 24 lines and a data bus of 8 lines, how much is the maximum capacity to manage memory?

[<$>] 16 MegaByte

Question 3 [<TB>]: In a memory structure of the form $2^N \times M$, which of the following statements is true?

[<$>] Memory consists of 2^N memory cells, each memory cell contains M bits

Question 4 [<KH>]: Given a computer with 4GB main memory capacity, 512KB cache memory capacity, 32byte line size, 1 byte memory compartment length. In the case of the direct mapping technique of Tag + Line + Word address form emitted by the processor to access the Cache is:

[<$>] 13+14+5

Question 5 [<TB>]: Cache memory works thanks to the principle:

[<$>] Memory Reference Localization

Question 6 [<TB>]: With an SRAM memory chip with n address lines and m data lines, the chip's capacity is:

[<$>] $2^n \times m$ bits

Question 7 [<DE>]: Considering the Cache memory, which of the following address mapping techniques are available?

[<$>] Direct, Full Link, Aggregate Link

Question 8 [<KH>]: With a SRAM memory chip with an address bus of 32 lines and a data bus of 16 lines, how much is the maximum capacity to manage memory?

[<$>] 8 GigaByte

Question 9 [<DE>]: Main memory is usually composed of which of the following memory elements?

[<$>] DRAM

Question 10 [<DE>]: Characteristics of RAM in general

[<$>] Allows writing data

Question 11 [<TB>]: What is the structure of a DRAM memory cell?

[<$>] Consists of a capacitor and a Transistor

Question 12 [<TB>]: For the method of writing data to Cache, which of the following statements is false?

[<$>] Write-back is slow because it has to find out if the corresponding Block in the Cache has been replaced or not.

Question 13 [<DE>]: For RAM memory, which of the following statements is false:

[<$>] Is a non-volatile memory type

Question 14 [<KH>]: Given an SRAM memory chip with a memory capacity of 64K x 8bit, which of the following statements is true?

[<$>] Address lines from A_0 -> A_{15}

Question 15 [<DE>]: In modern computers, which of the following memory devices usually has the largest capacity?

[<$>] Hard Drive

Question 16 [<TB>]: Which of the following statements about PROM is true?

[<$>] Requires a dedicated device to record with the program, the data cannot be erased by the user

Question 17 [<TB>]: For ROM memory, which of the following is not true?

[<$>] Always has more capacity than RAM

Question 18 [<TB>]: Compared with internal memory, the computer's external memory has the following advantages:

   [<$>] Low cost per memory bit

Question 19 [<TB>]: Which of the following memories requires periodic refresh?

   [<$>] DRAM

Question 20 [<TB>]: The characteristics of Cache memory are:

   [<$>] Allows faster access than DRAM memory

Question 21 [<TB>]: In terms of functions, a computer memory system can have the following locations:

   [<$>] Inside CPU (registers), internal memory, external memory

Question 22 [<TB>]: In terms of computer memory system hierarchy, which of the following statements is false?

   [<$>] The register level is the slowest exchange level

Question 23 [<DE>]: ROM memory is memory:

   [<$>] Read data only

Question 24 [<DE>]: Which of the following is a variable memory?

   [<$>] RAM

Question 25 [<KH>]: For a computer with 512MB main memory capacity, 128KB Cache memory capacity, 16byte line size, 2byte memory compartment length. In the case of a full link mapping technique in the form of Tag + Word addresses emitted by the processor to access the Cache is:

   [<$>] 25+3

Question 26 [<TB>]: The capacity of memory is determined by

   [<$>] Number of bits or words that memory can store

Question 27 [<TB>]: For ROM memory, which of the following statements is true:

   [<$>] Made from Transistor or diode

Question 28 [<TB>]: In the association-set mapping technique, the address fields are:

[<$>] Tag + Set + Word

Question 29 [<TB>]: For cache memory, which of the following statements is true?

[<$>] Cache can be placed on the same chip as the CPU

Question 30 [<KH>]: Given the SRAM memory chip has the signals A_0 -> A_{13}, D_0 -> D_{15}, RD, WR, which of the following statements is false?

[<$>] WE is the data read control signal

Question 31 [<TB>]: Which of the following is not an advantage of external memory compared to the main memory of a computer:

[<$>] Memory access speed is usually very high

Question 32 [<TB>]: Given an SRAM memory chip with a memory capacity of 16K x 8bit, which of the following statements is true?

[<$>] There are 14 address lines

Question 33 [<KH>]: Given a computer with 128MB main memory capacity, 64KB Cache memory capacity, 16byte Line size, 1byte memory compartment length, 4Line Set size. In the case of Tag + Set + Word address set association mapping technique emitted by the processor to access the Cache is:

[<$>] 13+10+4

Question 34 [<TB>]: In the exchange between Cache and main memory, which of the following statements is false?

[<$>] Main memory divided into memory lines

Question 35 [<TB>]: With a SRAM memory chip with an address bus of 24 lines and a data bus of 16 lines, how much is the maximum capacity to manage memory?

[<$>] 32 MegaByte

Question 36 [<DE>]: What type of memory is the BIOS program stored in?

[<$>] ROM

Question 37 [<TB>]: In the full link mapping technique, the address fields are:

[<$>] Tag + Word

Question 38 [<TB>]: What is the structure of an SRAM memory cell?

[<$>] Is a flip-flop circuit consisting of six Transistors

Question 39 [<TB>]: In modern computers, which of the following memory devices has the smallest access time?

[<$>] Cache

Question 40 [<TB>]: For ROM memory, which of the following statements is true:

[<$>] EPROM is a type of ROM that can be erased and rewritten many times

Question 41 [<DE>]: Regarding the method of accessing the memory system, which of the following statements is false?

[<$>] Sequential Access to Cache

Question 42 [<DE>]: Which of the following statements about EPROM is true?

[<$>] User can erase data by device using ultraviolet light and charge data electrically

Question 43 [<KH>]: For cache memory, which of the following statements is true?

[<$>] Data transfer between CPU and Cache in memory word units

Question 44 [<TB>]: Which of the following statements is correct?

[<$>] Cache memory is faster than internal memory

Question 45 [<TB>]: An advantage of external memory compared to a computer's internal memory is:

[<$>] Large capacity

Question 46 [<KH>]: Considering the hierarchy of computer memory systems, which of the following statements is true?

[<$>] From external memory to diminishing capacity register

Question 47 [<TB>]: For RAM memory, which of the following statements is true:

[<$>] Is a place to store information that the computer is processing

Question 48 [<KH>]: Given a computer with 512MB main memory capacity, 128KB Cache memory capacity, 32byte Line size, 2byte memory compartment length, 4Line Set size. In the case of Tag + Set + Word address set association mapping technique emitted by the processor to access the Cache is:

[<$>] 14+10+4

Question 49 [<TB>]: With an SRAM memory chip with an address bus of 15 lines and a data bus of 8 lines, how much is the maximum capacity to manage memory?

[<$>] 32 KiloByte

Question 50 [<DE>]: What are the characteristics of ROM memory ?

[<$>] Content is not changed

Question 51 [<DE>]: What types of memory access are there?

[<$>] There are four types of memory access: Sequential Access, Direct Access, Random Access, and Linked Access.

Question 52 [<KH>]: For the method of writing data to Cache, which of the following statements is true?

[<$>] Write-back write speed is fast because only write to Cache, when the corresponding block in Cache is replaced, the whole block is returned to main memory.

Question 53 [<KH>]: Given a computer with 4GB main memory capacity, 512KB Cache memory capacity, 32byte Line size, 4byte memory compartment length. In the case of a full link mapping technique in the form of Tag + Word addresses emitted by the processor to access the Cache is:

[<$>] 27+3

Question 54 [<TB>]: For random access memory, which of the following is true?

[<$>] Memory data is read or written at random times

Question 55 [<TB>]: For Cache memory, considering the direct mapping technique, the order to find Block in the cache is done based on the fields in the address emitted by the CPU as follows:

[<$>] Line -> Tag -> Word

Question 56 [<KH>]: Given a computer with 512MB main memory capacity, 128KB Cache memory capacity, 16byte line size, 4byte memory compartment length. In the case of a full link mapping technique in the form of Tag + Word addresses emitted by the processor to access the Cache is:

[<$>] 24+2

Question 57 [<TB>]: For computer main memory, which of the following statements is false?

[<$>] Contains programs and data in the form of libraries

Question 58 [<KH>]: Given a computer with 128MB main memory capacity, 64KB Cache memory capacity, Line size 8bytes, memory compartment length 1byte. In the case of the direct mapping technique of Tag + Line + Word address form emitted by the processor to access the Cache is:

[<$>] 11+13+3

Question 59 [<DE>]: Features of SRAM

[<$>] No cyclic refresh

Question 60 [<TB>]: Given an SRAM memory chip with a memory capacity of 64K x 8bit, which of the following statements is true? wrong?

[<$>] There are 14 address lines

[<$>] There are 24 address lines and 8 data lines

Question 61 [<TB>]: Given an SRAM memory chip with a memory capacity of 64K x 8bit, which of the following statements is false?

[<$>] There are 8 address lines and 16 data lines

Question 62 [<DE>]: Flash Disk memory is memory of the form:

[<$>] Ultra-fast semiconductor memory

Question 63 [<TB>]: Given the SRAM memory chip has the signals A_0 -> A_{13}, D_0 -> D_{15}, RD, WR, which of the following statements is false?

[<$>] Chip capacity is 16KB

Question 64 [<TB>]: What is the function of the cache memory in the computer?

[<$>] Stores data frequently used by the processor

Question 65 [<DE>]: With an SRAM memory chip with an address bus of 20 lines and a data bus of 8 lines, how much is the maximum capacity for memory management?

[<$>] 1 MegaByte

Question 66 [<KH>]: Of the SRAM and DRAM memories, which one consumes more power?

[<$>] SRAM

Question 67 [<TB>]: Which of the following statements is correct?

[<$>] SRAM memory used for Cache

Question 68 [<TB>]: How is the access speed of SRAM memory compared to DRAM memory?

[<$>] Faster

Question 69 [<TB>]: In modern computers, which of the following memory devices has the lowest access speed?

[<$>] Hard Drive

Question 70 [<KH>]: Given a computer with 256MB main memory capacity, 128KB Cache memory capacity, 32byte line size, 4byte memory compartment length. In the case of a full link mapping technique in the form of Tag + Word addresses emitted by the processor to access the Cache is:

[<$>] 23+3

Question 71 [<DE>]: For ROM memory, which of the following is true?

[<$>] Random access memory

Question 72 [<KH>]: With a DRAM memory chip with a 15-way address bus and a 16-way data bus, how much is the maximum capacity to manage memory?

[<$>] 64 KiloByte

Question 73 [<TB>]: Given the SRAM memory chip has signals A_0 -> A_{13}, D_0 -> D_{15}, RD, WR, which of the following statements is false?

[<$>] RD is data write control signal

Question 74 [<TB>]: Considering the Cache memory, each Line is appended with a Tag to:

[<$>] Determines which block of main memory is in the Line

Question 75 [<DE>]: For computer main memory, which of the following statements is true?

[<$>] Processor-addressed computer memory

Question 76 [<KH>]: With an SRAM memory chip with an address bus of 32 lines and a data bus of 8 lines, how much is the maximum capacity for memory management?

[<$>] 4 GigaByte

Question 77 [<TB>]: Compared with internal memory, the computer's external memory has the following advantages:

[<$>] No data loss when power off

Question 78 [<DE>]: For ROM memory, which of the following statements is false:

[<$>] Is a type of variable memory

Question 79 [<DE>]: For a computer memory system, which of the following statements is not a physical property?

[<$>] Read-only memory

Question 80 [<TB>]: In modern computers, which of the following memory devices usually has the smallest capacity?

[<$>] Cache

Question 81 [<DE>]: In the direct mapping technique, the address fields are:

[<$>] Tag + Line + Word

Question 82 [<DE>]: Which of the following statements about Maskable ROM is true?

[<$>] The data is pre-loaded by the manufacturer, the data cannot be erased by the user

Question 83 [<KH>]: Given a computer with 4GB main memory capacity, 512KB Cache memory capacity, 32byte Line size, 1byte memory compartment length, 4Line Set size. In the case of Tag + Set + Word address set association mapping technique emitted by the processor to access the Cache is:

[<$>] 15+12+5

Question 84 [<TB>]: When the CPU accesses the Cache memory, the following two possibilities occur:

[<$>] There is data in the Cache, or there is no data in the Cache

Question 85 [<DE>]: The characteristics of Cache memory are:

[<$>] Small access time

Question 86 [<TB>]: For RAM memory, which of the following statements is false:

[<$>] DRAM is made from flipping circuit

Question 87 [<TB>]: Characteristics of DRAM

[<$>] Must be periodically refreshed

Question 88 [<TB>]: For Cache memory, considering the association-set mapping technique, the order to find Block in the cache is performed based on the fields in the address emitted by the CPU as follows:

[<$>] Set -> Tag -> Word

Question 89 [<KH>]: Given a computer with 265MB main memory capacity, 128KB Cache memory capacity, 16byte line size, 2byte memory compartment length. In the case of the direct mapping technique of Tag + Line + Word address form emitted by the processor to access the Cache is:

[<$>] 11+13+3

Question 90 [<DE>]: Which of the following statements about EEPROM is true?

[<$>] User can load or delete data electrically

Question 91 [<KH>]: Given a SRAM memory chip with a memory capacity of 16K x 8bit, which of the following statements is true?

[<$>] Data lines from D_0 -> D_7

Question 92 [<KH>]: Given a computer with 256MB main memory capacity, 128KB cache memory capacity, 128byte Line size, 4byte memory compartment length, 8Line Set size. In the case of Tag + Set + Word address set association mapping technique emitted by the processor to access the Cache is:

[<$>] 14+7+5

Question 93 [<KH>]: Given an SRAM memory chip with a memory capacity of 64K x 8bit, which of the following statements is true?

[<$>] Data lines from D_0 -> D_7

Question 94 [<KH>]: With a SRAM memory chip with an address bus of 20 lines and a data bus of 16 lines, how much is the maximum capacity to manage memory?

[<$>] 2 MegaByte

Question 95 [<TB>]: Given the SRAM memory chip has the signals A_0 -> A_7, D_0 -> D_7, RD, WR, which of the following statements is true?

[<$>] The capacity of the chip is 256B

Question 96 [<DE>]: In terms of physical type, what types of memory are there?

[<$>] Semiconductor memory, magnetic memory, optical memory

Question 97 [<TB>]: For random access memory, which of the following is not true?

[<$>] Access time to any cell in memory is the same

Question 98 [<TB>]: ROM BIOS does not contain which of the following programs?

[<$>] System Configuration Information

Question 99 [<DE>]: Which of the following memories allows random access?

[<$>] Semiconductor memory (RAM, ROM, ...)

[(<002611_C6>)] , , Ring 6

Sentence 1 [<DE>]: DMA stands for:

[<$>] Direct Memory Access

Question 2 [<TB>]: Features of multi-level centralized bus arbitration:

[<$>] Peripherals connected to different Bus request lines

Question 3 [<TB>]: With the program I/O method, which of the following statements is false?

[<$>] Peripheral device is an active object in data exchange

Question 4 [<TB>]: What is the important feature of Asynchronous Bus?

[<$>] No common clock signal controlling operation

Question 5 [<TB>]: For block DMA, which of the following statements is true?

[<$>] After transmitting the whole data block, DMA returns the bus to the CPU

Question 6 [<DE>]: How many methods are there to determine the interrupt module ?

[<$>] 4 methods

Question 7 [<TB>]: For serial I/O concatenation, which of the following statements is true?

[<$>] A converter from parallel to serial data and/or vice versa is required

Question 8 [<DE>]: Which of the following is part of a peripheral device?

[<$>] Signal Converter

Question 9 [<TB>]: The main components in the I/O system

[<$>] Peripherals and I/O modules

Question 10 [<TB>]: In what type of Bus arbitration are peripheral devices connected to different Bus request lines?

[<$>] Multi-level centralized bus arbitration

Question 11 [<TB>]: With the software round-check method (in determining the interrupt modulus), which of the following statements is false?

[<$>] CPU checks multiple I/O modules at the same time

Question 12 [<TB>]: Modem is a type of peripheral device:

[<$>] Communication

Question 13 [<KH>]: Which I/O control method does the CPU have to regularly check the status of peripheral devices?

[<$>] Program I/O method

Question 14 [<KH>]: Compared with the synchronous bus, the asynchronous bus has the following characteristics:

[<$>] If one master-slave pair is slow, the next master-slave pair is not affected.

Question 15 [<TB>]: The data bus in the computer is:

[<$>] Bidirectional bus with each line

Question 16 [<DE>]: Which of the following is a component of the I/O module?

[<$>] Status/control register

Question 17 [<TB>]: The printer is a peripheral device:

[<$>] Human-machine interface

Question 18 [<TB>]: For transparent DMA, which of the following statements is true?

[<$>] When the CPU is not using the Bus, take advantage of DMA

Question 19 [<DE>]: The system bus of a computer includes:

[<$>] Data Bus, Address Bus and Control Bus

Question 20 [<KH>]: In which cases should synchronous bus be used?

[<$>] Almost all operations have a processing time equal to a multiple of Bus cycles

Question 21 [<TB>]: What is the function of the Expansion Bus in a computer?

[<$>] Connect the I/O system to the microprocessor

Question 22 [<TB>]: With DMA I/O, which of the following statements is true?

[<$>] Add hardware module on Bus

Question 23 [<DE>]: Which parameter characterizes the data transfer rate on the Bus?

[<$>] Frequency of Bus

Question 24 [<TB>]: How many address lines does the IBM PC bus have?

[<$>] 20 lines

Question 25 [<TB>]: Which bus in the computer is responsible for connecting the processor to the main memory?

[<$>] System Bus

Question 26 [<TB>]: For parallel input and output concatenation, which of the following statements is false?

[<$>] Sequential transmission bit by bit

Question 27 [<TB>]: For parallel input and output concatenation, which of the following statements is true?

[<$>] Fast Speed

Question 28 [<TB>]: For DMA data interchange, which of the following statements is true?

[<$>] This method is suitable for exchanging large array data

Question 29 [<TB>]: What is the function of Bus Arbitration?

[<$>] Bus master dispute resolution

Question 30 [<TB>]: With the program I/O method, which of the following statements is true?

[<$>] This is the simplest data exchange method

Question 31 [<TB>]: For parallel input and output concatenation, which of the following statements is false?

[<$>] Less data transmission required

Question 32 [<TB>]: For parallel input and output concatenation, which of the following statements is true?

[<$>] Needs multiple data lines

Question 33 [<TB>]: Network Interface Card (NIC) is a type of peripheral device:

[<$>] Communication

Question 34 [<TB>]: For block DMA, which of the following statements is false?

[<$>] Intermittent transfer in groups of 2 bytes of data

Question 35 [<DE>]: Which of the following is not an I/O module?

[<$>] Data Buffer

Question 36 [<DE>]: Which of the following is a peripheral device component?

[<$>] Data Buffer

Question 37 [<DE>]: Which parameter indicates the number of Bytes transferred to the Bus in a unit of time?

[<$>] Bus Bandwidth

Question 38 [<KH>]: Which component can play the role of Bus Master?

[<$>] CPU or IO chips can act as Bus master

Question 39 [<TB>]: Scanner is a type of peripheral device:

[<$>] Human-machine interface

Question 40 [<KH>]: What does the DMA mechanism allow to do?

[<$>] Direct data transfer between main memory and I/O modules

Question 41 [<KH>]: In which type of Bus arbitration, the division of the right to use the Bus is undertaken by a single Bus arbitration unit?

[<$>] Centralized Bus Referee

Question 42 [<KH>]: What is the function of the System Bus in a computer?

[<$>] Connect the microprocessor to main memory, L3 cache, and I/O pairing controllers

Question 43 [<KH>]: With the hardware round check method (in determining the interrupt modulus), which of the following statements is false?

[<$>] The system has multiple priority interrupt request lines

Question 44 [<KH>]: Which of the following characteristics is not a synchronous bus?

[<$>] Data exchange between devices requires handshake signal

Question 45 [<TB>]: What is the function of the Bus system in a computer?

[<$>] Linking computer components

Question 46 [<TB>]: What is the function of the Microprocessor Bus in a computer?

[<$>] Transmission path between CPU and L2 Cache

Question 47 [<TB>]: For serial I/O concatenation, which of the following statements is false?

[<$>] Transmit multiple bits at once

Question 48 [<TB>]: How many data lines does the IBM PC bus have?

[<$>] 8 lines

Question 49 [<TB>]: Methods of determining interrupt module include

[<$>] Using multiple interrupt request lines, software polling, hardware polling, using interrupt controller

Question 50 [<TB>]: Features of centralized bus arbitration:

[<$>] The division of the right to use the Bus is done by a single bus arbitration unit

Question 51 [<KH>]: With the DMA I/O method, which of the following statements is false?

[<$>] CPU and DMAC combined data exchange control

Question 52 [<KH>]: In the case of using a synchronous bus, if an operation has a completion time of 3.2 cycles, in how many cycles will it actually be performed?

[<$>] 4

Question 53 [<KH>]: For transparent DMA, which of the following statements is false?

[<$>] When DMAC does not use Bus, CPU uses Bus

Question 54 [<TB>]: With interrupt I/O, which of the following statements is true?

[<$>] Is a method of processing by both hardware and software

Question 55 [<TB>]: Bus width is determined by:

[<$>] Bus data line number

Question 56 [<TB>]: The functions of peripheral devices are:

[<$>] Converts data between inside and outside the computer

Question 57 [<TB>]: What is the input/output control method that the CPU, when receiving the ready signal of the peripheral device, will have to pause the work it is doing to exchange data with the peripheral device?

[<$>] Interrupt I/O method

Question 58 [<TB>]: The address bus in the computer is:

[<$>] One way bus

Question 59 [<TB>]: With DMA I/O, which of the following statements is true?

[<$>] A non-CPU-controlled method of exchanging data

Question 60 [<TB>]: In which type of bus arbitration, the division of the right to use the bus does not need a separate bus arbitration unit

[<$>] Bus referee is not focused

Question 61 [<TB>]: With interrupt I/O, which of the following statements is false?

[<$>] CPU must wait for the ready state of the peripheral by the check instruction in the program

Question 62 [<KH>]: Why is the synchronous bus more widely used in practice than the asynchronous bus?

[<$>] Synchronous bus systems are easier to design

Question 63 [<TB>]: For a periodized DMA, which of the following statements is true?

[<$>] CPU and DMAC interleave using Bus

Question 64 [<TB>]: With the interrupt request multipath method (in determining the interrupt module), which of the following statements is true?

[<$>] CPU must have different interrupt request lines for each I/O module

Question 65 [<TB>]: For serial I/O concatenation, which of the following statements is false?

[<$>] Fast Speed

Question 66 [<DE>]: Which of the following is a component of the I/O module?

[<$>] I/O ports

Question 67 [<DE>]: The keyboard is a type of peripheral device:

[<$>] Human-machine interface

Question 68 [<TB>]: What frequency does the IBM PC bus operate on?

[<$>] 4.77Mhz

Question 69 [<KH>]: For the I/O control method, which of the following is not a characteristic of interrupt I/O?

[<$>] CPU must wait for I/O module

Question 70 [<DE>]: Which of the following is not a peripheral device?

[<$>] I/O ports

Question 71 [<TB>]: What is the input/output control method where the CPU does not have to directly control the data exchange process?

[<$>] Direct memory access I/O method

Question 72 [<TB>]: Typical bus frequency for:

[<$>] Bus data transfer rate

Question 73 [<TB>]: The control bus in the computer is:

[<$>] One-way bus for each line, two-way for the whole Bus

Question 74 [<DE>]: Which of the following is not an I/O module?

[<$>] Data Converter

Question 75 [<DE>]: Optical drive is a type of peripheral device:

[<$>] Machine-to-machine communication

Question 76 [<KH>]: For DMA data interchange, which of the following statements is true?

[<$>] This is a purely hardware exchange method

Question 77 [<TB>]: Which bus in the computer is responsible for the transmission between the CPU and the L2 Cache memory?

[<$>] Processor Bus

Question 78 [<KH>]: In the case of using the Asynchronous Bus, if an operation has a completion time of 3.2 cycles, in how many cycles will it actually be performed?

[<$>] 3.2

Question 79 [<TB>]: What is the function of the Bus in a computer's microprocessor?

[<$>] Is the transmission line between the blocks of the processor

Question 80 [<KH>]: With the DMA I/O method, which of the following statements is false?

[<$>] This is a slow data exchange method

Question 81 [<DE>]: Which bus parameter indicates its line?

[<$>] Bus width

Question 82 [<KH>]: It is not possible to connect a peripheral device directly to the System Bus because (please point out which is incorrect):

[<$>] Manufacturers cannot make devices that connect directly between the microprocessor and peripherals

Question 83 [<TB>]: What is the important feature of the synchronous bus?

[<$>] There is a common clock signal that controls the operation

Question 84 [<TB>]: For parallel input and output concatenation, which of the following statements is false?

[<$>] Parallel to serial data converter and/and vice versa

Question 85 [<DE>]: For serial I/O concatenation, which of the following statements is true?

[<$>] Sequential transmission bit by bit

Question 86 [<TB>]: With the program I/O method, which of the following statements is true?

[<$>] It is a completely software-based method

Question 87 [<TB>]: Features of non-centralized Bus arbitration with multibus:

[<$>] The division of Bus usage rights does not require a separate Bus arbitration unit

Question 88 [<TB>]: With interrupt I/O, which of the following statements is true?

[<$>] Peripheral device is an active object in data exchange

Question 89 [<DE>]: For parallel input and output concatenation, which of the following statements is true?

[<$>] Transmit multiple bits at once

Question 90 [<DE>]: For serial I/O concatenation, which of the following statements is true?

[<$>] Less data transmission required

Question 91 [<KH>]: Which bus in the computer is responsible for the transmission line between the blocks of the microprocessor?

[<$>] Bus in microprocessor

Question 92 [<DE>]: For a periodical DMA, which of the following statements is false?

[<$>] DMAC uses Bus completely

Question 93 [<TB>]: In some processors that have an I/O address space, which of the following is associated with the I/O addresses?

[<$>] Each I/O address is associated with an I/O port

Question 94 [<DE>]: Which of the following is a component of the I/O module?

[<$>] Data buffer register

Question 95 [<TB>]: Features of single-level centralized bus arbitration:

[<$>] Peripherals sharing a line request Bus

Question 96 [<DE>]: The monitor is a type of peripheral device:

[<$>] Human-machine interface

Question 97 [<DE>]: Which of the following is not a peripheral device?

[<$>] Peripheral device control/status register

Question 98 [<KH>]: With the DMA I/O method, which of the following statements is false?

[<$>] When the DMAC has finished controlling the data exchange it does not need to notify the CPU

Question 99 [<KH>]: Basic operations in the I/O system

[<$>] Data in and data out

Question 100 [<KH>]: Which bus in the computer is responsible for connecting input and output devices to the microprocessor?

[<$>] Expansion Bus

Question 101 [<DE>]: What is the DMA mechanism?

[<$>] Direct memory access

Question 102 [<KH>]: Compared with asynchronous bus, synchronous bus has the following characteristics:

[<$>] It's easier to control the operation of the computer

Question 103 [<KH>]: In what cases should asynchronous bus be used?

[<$>] When the system has many devices with huge difference in speed

Question 104 [<DE>]: Which of the following buses is a one-way bus?

[<$>] Address Bus

Question 105 [<DE>]: For serial I/O concatenation, which of the following statements is false?

[<$>] Needs multiple data lines

Question 106 [<DE>]: Hard disk drive is a type of peripheral device:

[<$>] Machine-to-machine communication

Question 107 [<KH>]: With the software round check method (in determining the interrupt modulus), which of the following statements is true?

[<$>] CPU executes software asking each I/O module in turn

Question 108 [<DE>]: How many lines does the IBM PC bus have?

[<$>] 62 lines

Question 109 [<DE>]: There are the following types of DMA data exchange:

[<$>] Block DMA, Cycle DMA, Transparent DMA

Question 110 [<DE>]: Bus bandwidth is determined by:

[<$>] Number of Bytes transferred to the Bus in a unit of time (sec)

Question 111 [<KH>]: For DMA data interchange, which of the following statements is true?

[<$>] This is the fastest exchange method

Question 112 [<TB>]: How many types of peripheral device pairing are there?

[<$>] 2 styles

Question 113 [<TB>]: Which of the following buses is a bidirectional bus for each signal line?

[<$>] Data Bus

Question 114 [<KH>]: One of the characteristics of the synchronous bus is:

[<$>] All operations are performed in times that are multiples of Bus cycles

Question 115 [<KH>]: There are three methods of I/O control as follows:

[<$>] I/O by program, by interrupt, by DMA

Question 116 [<KH>]: In which type of Bus arbitration do peripheral devices share a bus request line?

[<$>] One level centralized bus referee

[(<002611_C7>)] , , Ring 7

Question 1 [<TB>]: Intel 80186/80286 processor with architecture is

[<$>] 4-bit

[<$>] 32-bit

[<$>] 16-bit

[<$>] 8-bit

Question 2 [<TB>]: Which of the following computers are capable of handling floating point:

[<$>] 80386

[<$>] 80286

[<$>] 80186

[<$>] 80486

Question 3 [<KH>]: At the microarchitecture level, the PUSH instruction performs the operation (note: ac (accumulator); sp (stack pointer); m (memory))

[<$>] sp:=sp-1; m[sp]:=ac

[<$>] m[ac]:=m[sp]; sp:=sp+1

[<$>] sp:=sp-1; m[sp]:=m[ac]

[<$>] ac:=m[sp]; sp:=sp+1

Question 4 [<DE>]: Intel 8008/8080 processor with architecture is

[<$>] 4-bit

[<$>] 8-bit

[<$>] 16-bit

[<$>] 32-bit

Question 5 [<KH>]: At the microarchitecture level, the LODL instruction performs the operation (note: ac (accumulator); sp (stack pointer); m (memory); x (address value))

[<$>] ac:=m[sp+x]

[<$>] ac:=m[x]

[<$>] m[x]:=ac

[<$>] m[sp+x]:=ac

Question 6 [<KH>]: At the microarchitecture level, the JPOS instruction performs the operation (note: ac (accumulator); pc (program counter); x (address value))

[<$>] if ac=0 then pc:=x

[<$>] if ac <> 0 then pc:=x

[<$>] if ac < 0 then pc:=x

[<$>] if ac ≥ 0 then pc:=x

Question 7 [<KH>]: At the microarchitecture level, the SUBD instruction performs an operation (note: ac (accumulator); sp (stack pointer); m (memory); x (address value))

[<$>] ac:=ac+m[sp+x]

[<$>] ac:=ac-m[sp+x]

[<$>] ac:=ac-m[x]

[<$>] ac:=ac+m[x]

Question 8 [<TB>]: At the microarchitecture level, the JNZE instruction performs the operation (note: ac (accumulator); pc (program counter); x (address value))

[<$>] if ac ≥ 0 then pc:=x

[<$>] if ac < 0 then pc:=x

[<$>] if ac=0 then pc:=x

[<$>] if ac <> 0 then pc:=x

Question 9 [<TB>]: Intel Celeron processor architecture is

[<$>] 64-bit

[<$>] 8-bit

[<$>] 16-bit

[<$>] 32-bit

Question 10 [<TB>]: Intel 80386/80486 processor architecture is

[<$>] 8-bit

[<$>] 16-bit

[<$>] 32-bit

[<$>] 64-bit

Question 11 [<TB>]: At the microarchitecture level, the LODD instruction performs the operation (note: ac (accumulator); sp (stack pointer); m (memory); x (address value))

[<$>] m[sp+x]:=ac

[<$>] ac:=m[sp+x]

[<$>] m[x]:=ac

[<$>] ac:=m[x]

Question 12 [<TB>]: At the microarchitecture level, the JNEG instruction performs an operation (note: ac (accumulator); pc (program counter); x (address value))

[<$>] if ac < 0 then pc:=x

[<$>] if ac ≥ 0 then pc:=x

[<$>] if ac=0 then pc:=x

[<$>] if ac <> 0 then pc:=x

Question 13 [<TB>]: At the microarchitecture level, the ADDL instruction performs the operation (note: ac (accumulator); sp (stack pointer); m (memory); x (address value))

[<$>] ac:=ac-m[x]

[<$>] ac:=ac+m[x]

[<$>] ac:=ac-m[sp+x]

[<$>] ac:=ac+m[sp+x]

Question 14 [<KH>]: At the microarchitecture level, the STOL instruction performs the operation (note: ac (accumulator); sp (stack pointer); m (memory); x (address value))

[<$>] m[x]:=ac

[<$>] ac:=m[x]

[<$>] m[sp+x]:=ac

[<$>] ac:=m[sp+x]

Question 15 [<KH>]: At the microarchitecture level, the PSHI instruction performs the operation (note: ac (accumulator); sp (stack pointer); m (memory))

[<$>] sp:=sp-1; m[sp]:=m[ac]

[<$>] m[ac]:=m[sp]; sp:=sp+1

[<$>] sp:=sp-1; m[sp]:=ac

[<$>] ac:=m[sp]; sp:=sp+1

Question 16 [<KH>]: At the microarchitecture level, the POP instruction performs the operation (note: ac (accumulator); sp (stack pointer); m (memory))

[<$>] sp:=sp-1; m[sp]:=m[ac]

[<$>] m[ac]:=m[sp]; sp:=sp+1

[<$>] sp:=sp-1; m[sp]:=ac

[<$>] ac:=m[sp]; sp:=sp+1

Question 17 [<TB>]: Intel 8085 processor architecture is

[<$>] 4-bit

[<$>] 8-bit

[<$>] 16-bit

[<$>] 32-bit

Question 18 [<DE>]: Which of the following computers is capable of floating point processing (choose the most correct answer):

[<$>] 80386/80486

[<$>] 80486

[<$>] 80486/Celeron

[<$>] 80486/Pentium/Celeron

Question 19 [<TB>]: Intel Pentium III, Pentium 4 processors have the architecture of

[<$>] 64-bit

[<$>] 8-bit

[<$>] 16-bit

[<$>] 32-bit

Question 20 [<TB>]: At the microarchitecture level, the JZER instruction performs an operation (note: ac (accumulator); pc (program counter); x (address value))

[<$>] if ac <> 0 then pc:=x

[<$>] if ac=0 then pc:=x

[<$>] if ac ≥ 0 then pc:=x

[<$>] if ac < 0 then pc:=x

Question 21 [<TB>]: At the microarchitecture level, the SUBL instruction performs the operation (note: ac (accumulator); sp (stack pointer); m (memory); x (address value))

[<$>] ac:=ac+m[sp+x]

[<$>] ac:=ac-m[sp+x]

[<$>] ac:=ac+m[x]

[<$>] ac:=ac-m[x]

Question 22 [<TB>]: At the microarchitecture level, the ADDD instruction performs the operation (note: ac (accumulator); sp (stack pointer); m (memory); x (address value))

[<$>] ac:=ac-m[sp+x]

[<$>] ac:=ac+m[sp+x]

[<$>] ac:=ac-m[x]

[<$>] ac:=ac+m[x]

Question 23 [<TB>]: At the microarchitecture level, the STOD instruction performs the operation (note: ac (accumulator); sp (stack pointer); m (memory); x (address value))

[<$>] m[x]:=ac

[<$>] ac:=m[x]

[<$>] m[sp+x]:=ac

[<$>] ac:=m[sp+x]

Question 24 [<DE>]: Intel 4004 processor architecture is

[<$>] 4-bit

Question 25 [<DE>]: Intel Pentium, Pentium II processors have the architecture of

[<$>] 32-bit

Question 26 [<DE>]: Intel 8086/8088 processor architecture is

[<$>] 16-bit

Question 27 [<DE>]: Which of the following computers cannot handle floating point:

[<$>] 80386

Question 28 [<DE>]: Intel Itanium processor architecture is

[<$>] 64-bit

Question 29 [<TB>]: At the microarchitecture level, the POPI instruction performs the operation (note: ac (accumulator); sp (stack pointer); m (memory))

[<$>] m[ac]:=m[sp]; sp:=sp+1